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An Ultra-Wideband Low Noise Amplifier and Spectrum Sensing Technique for Cognitive Radio

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An ultra-wideband low noise amplifier and spectrum sensing technique for cognitive radio

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I would also like to thank my parents who supported me financially and emotionally throughout college and graduate school.

ABSTRACT

A low power ultra-wideband, inductorless low noise amplifier (LNA) employing a noise cancellation architecture and designed in a commercially available 40nm 1.2V digital CMOS process is presented. The amplifier targets cognitive radio communication applications which cover the frequency range of 1-10 GHz and achieves an S_{11} < -9.5 dB from 1.4 – 9.5 GHz. Within this bandwidth the maximum power gain is 13.4 dB, the maximum noise figure is 4.3 dB, and the miminum IIP3 is 0 dBm. The total power consumption of the LNA (neglecting the buffer required to drive the 50 Ω test equipment) is 8 mW. The total area consumed is 0.031mm^2 excluding the pads.

A spectrum sensing technique using translational loop technique is also proposed to realize simultaneous spectrum sensing and data reception of cognitive radio. This technique also eliminates the need for tunable sharp band-select filter at the front-end.

CHAPTER 1. INTRODUCTION

Upcoming applications in cognitive radios, multi-band/multi-standard radios and ultra-wideband (UWB) communication cover frequencies from 1GHz up to 10 GHz. Such applications will require the radio be able to operate from 1GHz to 10GHz. This means the low noise amplifier (LNA) used for the transceiver needs to have low noise figure, enough power gain, good input impedance matching and good linearity at radio frequencies up to 10 GHz. This thesis focuses on developing an ultra-wideband LNA and spectrum sensing technique for the cognitive radio front-end.

Over the years, people have tried various structures to achieve ultra-wideband operation. Using common-source topology will require building band-pass filters at the input which requires area-consuming reactive components like inductors and capacitors. Poor isolation between input and output node (gate and drain) of such topology will almost always require cascoding another MOSFET which is not favored with the downscaling of feature size due to lower supply voltage [1]-[5]. Use of active inductor will eliminate the use of any bulky passive inductor but the noise figures reported are high due the additional noise from active load devices [6]-[11]. Feedback techniques are well-known for their wideband characteristics but they still need the addition of inductors where multi-GHz of bandwidth is required [12]-[17].

Use of inductors not only occupies large area, they also require time-consuming customized design. In some cases, the effort needed to design one inductor is comparable to the rest of the circuitry. Inductors are sometimes used to compensate for parasitic capacitances at critical nodes. These parasitic capacitance values are constantly changing

with each new generation of process thus requiring a new design of the corresponding inductor. This makes it more time-consuming to migrate from one technology to another.

Another common technique used to build ultra-wideband LNAs is noise-cancellation. There are multiple ways to achieve noise-cancellation [18]-[20] but this work explores the use of purely inductorless noise-cancelling structure which is well suited for cognitive radio applications in all digital deep submicron technologies [21].

Cognitive radio is a technology that is intended to solve the problem of inefficient use of radio frequency spectrum [22]. But current spectrum sensing techniques use two separate RF front-ends in parallel; one for data reception and one for spectrum sensing [23]. This option requires large die area and power consumption associated with duplicating the entire RF front end. Combined with the need for two flexible band-select filters and a dedicated antenna for spectrum sensing, this solution is unfeasible for handheld mobile applications. This thesis proposes a novel spectrum sensing algorithm which eliminates the duplication of entire front-end and the use of multiple band-select filters.

The remainder of this thesis is organized as follows: Chapter 2 reviews the figure of merits associated with LNA design and how they trade-off with one another, Chapter 3 reviews the current state-of-the-art in the field of ultra-wideband LNA design, Chapter 4 reviews several other noise-cancelling achievements and the proposed design and simulation results are presented, in Chapter 5, cognitive radio will be discussed along with proposed spectrum sensing techniques and Chapter 6 discusses future of this project.

CHAPTER 2. LOW-NOISE AMPLIFIER

A low-noise amplifier (LNA) is normally used in the first stage of a receiver. As the name suggest, it is highly desirable that this stage introduces as little noise as possible while giving sufficient power gain to the weak signal picked up by the antenna. The reason for having low noise is as follows. Consider the noise figure of a cascaded system shown in Fig.1.

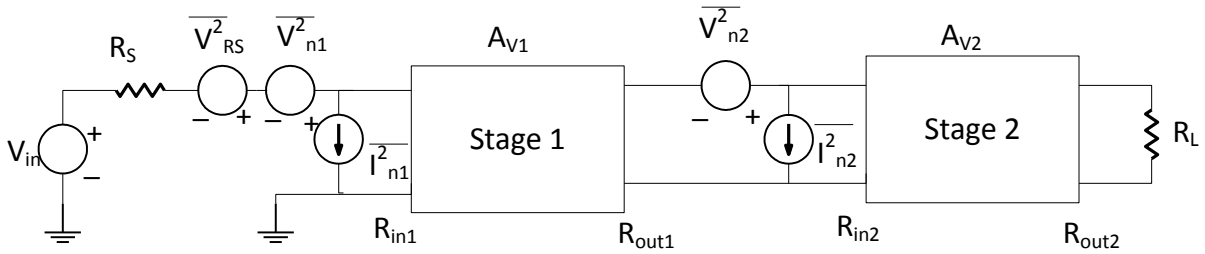

Figure 1. Cascaded noise stages.

The total noise figure of this two-stage system can be derived as [24]:

$$NF_{tot} = \frac{4kTR_S + \overline{(I_{n1}R_S + V_{n1})^2}}{4kTR_S} + \frac{\overline{(I_{n2}R_{out1} + V_{n2})^2}}{A_{v1}^2} \frac{1}{\left(\frac{R_{in1}}{R_S + R_{in1}}\right)^2} \frac{1}{4kTR_S} \quad (1)$$

In the above equation, k is Boltzmann constant, T is absolute temperature, R_{in1} and R_{out1} are the input and out resistance of the first stages, R_{in2} and R_{out2} are the input and out resistance of the second stage and R_S is source resistance. If we make the assumption that $R_S = R_{in1} = R_{out1} = R_{in2}$, (1) can be expressed in terms of noise figure of different stages as (2).

$$NF_{tot} = NF_1 + \frac{NF_2 - 1}{\alpha^2 A_{v1}^2} \quad (2)$$

Similarly, if we apply this to multiple stages, we can get [24]:

$$NF_{tot} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{p1}} + \cdots + \frac{NF_m - 1}{A_{p1} \ldots A_{p(m-1)}} \quad (3)$$

Equation (3) is also known as Friis formula which is named after the Danish-American electrical engineer Harald T. Friis [24]. From (3) we can see that the noise figure for any given certain stage is divided by the square of the power gain of the preceding stages. The result is that the total receiver noise figure is dominated by the first few stages, especially the very first one (namely the LNA). This is the rationale behind why the first stage amplifier needs to have as small of noise figure as possible.

Other than having a small noise figure, there are other performance metrics that are important. It is very important that the input impedance of the LNA is matched to a certain value, most commonly 50 Ω. A measure of the quality of the input match can be obtained by S_{11}. S_{11} is a member of scattering parameters (S-parameters) which are used to characterize linear electronic networks. This type of technique can be used when transistors are properly biased and linear small signal model is used for analysis [25]. If we assign the input port of an LNA to be port 1, S_{11} will be a complex number representing the ratio of how much power is reflected from port 1 to how much power is applied to port 1. So the magnitude of S_{11} (normally expressed in dB) is desired to be as small as possible (S_{11} = -∞ for a perfect impedance match). And the reason that it should be matched to 50 Ω is that most antennas have characteristic impedance of 50 Ω.

Another figure of merit that needs to be considered when designing an LNA is linearity. Non-linearity can cause problems such as gain compression, blocking and

intermodulation. One common way to quantify non-linearity is input-referred third-order intercept point (IIP3), normally expressed in dBm and is desired to be as high as possible.

Power consumption is another design specification that needs to be closely inspected. Considering only the noise performance and linearity can lead to biasing solution that makes the power consumption simply too big to be practically realized. Increased incorporation of RF systems into hand-held device makes it necessary to minimize power consumption in order to maximize battery life.

With each new generation of smaller feature sizes of CMOS process. Cost per unit area is constantly increasing. Thus area is another very important thing to consider in order to cut cost. Due to the large area that inductors consume and the large amount of time needed to design them, there has been a lot of research aimed at eliminating the use of inductors in RF systems.

As we can see, the design of an LNA is a multi-dimensional optimization problem. There are lots of trade-offs involved because the optimization of each individual specification does not arrive at the same sizing or biasing solution. This requires that the designer consider what is the best combination of performance specifications for the intended application of the LNA.

As an example, it will be shown why simultaneous maximum power gain and minimum noise figure can't be achieved. The equivalent noise model of a two port network is shown in Fig. 2.

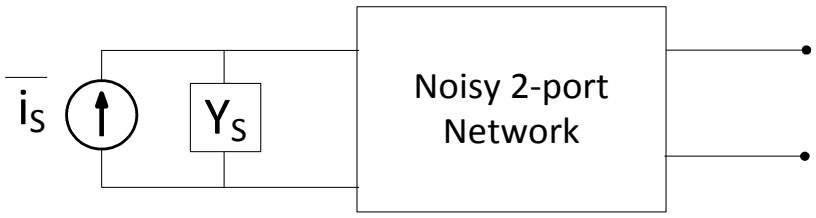

Figure 2. Noisy 2-port network driven by noisy source.

The input source is modeled as the parallel connection of an equivalent source admittance Y_S and noise current $\overline{i_s}$. The total noise contributed by the 2 port network is modeled as a noise voltage source $\overline{e_n}$ and a noise current source $\overline{i_n}$ (see Fig. 3) and the network is noiseless and linear. The goal is to find the optimum source admittance such that the minimum theoretical noise figure is achieved. After this derivation, we will see how the optimum source admittance for minimum noise figure differs from the optimum source admittance for maximum power transfer.

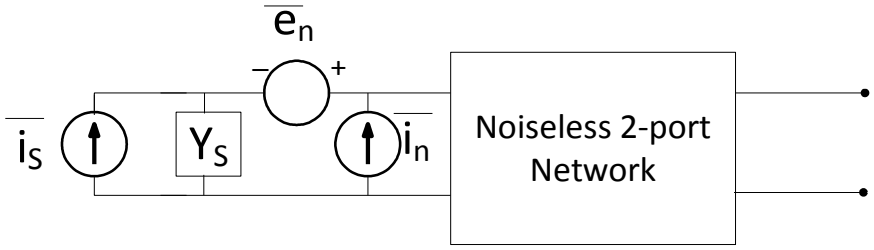

Figure 3. Equivalent noise model.

The definition of noise figure is expressed as:

$$NF = \frac{total\ output\ noise\ power}{output\ noise\ due\ to\ input\ source} \tag{4}$$

Although (4) is the definition and makes more intuitive sense, short-circuit mean-square current is used more often in calculations. The reason is that this method simplifies

calculation and is equivalent to power caculation because each individual power contribution is proportional to the short-circuit mean-square current with a proportional constant that is same for all the terms.

The noise figure of the system in Fig. 3 can be derived as:

$$NF = \frac{\overline{i_s^2} + \overline{|i_n + Y_s e_n|^2}}{i_s^2} \tag{5}$$

Equation (5) is derived under the assumption that there is no correlation between external noise source ($\overline{i_s}$) and internal noise sources ($\overline{e_n}$ and $\overline{i_n}$) which is a reasonable assumption. However, there normally is correlation between $\overline{e_n}$ and $\overline{i_n}$ and we model it as (6) and (7).

$$i_n = i_c + i_u \tag{6}$$

$$i_c = Y_c e_n \tag{7}$$

Equation (6) decomposes i_n into i_c which is correlated with e_n and i_u which is uncorrelated with e_n. Y_c is the correlation admittance that relates i_c and e_n. Now we can write (5) as (8).

$$NF = 1 + \frac{\overline{\left|i_u^2 + |Y_c + Y_s|^2 e_n^2\right|^2}}{i_s^2} \tag{8}$$

The noise voltage $\overline{e_n}$ and noise current $\overline{i_n}$ can be expressed in terms of an equivalent resistance or conductance respectively:

$$\overline{e_n^2} = R\ 4kT\Delta f \tag{9}$$

$$\overline{i_n^2} = G\ 4kT\Delta f \tag{10}$$

Using (9) and (10), (8) can be written as:

$$NF = 1 + \frac{G_u + |Y_c + Y_s|^2 R_n}{G_s} = 1 + \frac{G_u + \left[(G_c + G_s)^2 + (B_c + B_s)^2\right] R_n}{G_s} \tag{11}$$

The second part of (11) decomposes each admittance into a sum of conductance and susceptance (i.e. $Y_c = G_c + jB_c$). Now we can see that for any given noisy two port network, we can characterize it with four noise parameters: G_c, B_c, R_n and G_u. Now we can express the noise figure (see (8)) in terms of noise parameters:

$$NF = NF_{min} + \frac{R_n}{G_s}\left[\left(G_s - G_{opt}\right)^2 + \left(B_s - B_{opt}\right)^2\right] \tag{12}$$

where

$$NF_{min} = 1 + 2R_n\left[\sqrt{\frac{G_u}{R_n} + G_c^2} + G_c\right] \tag{13}$$

$$B_{opt} = -B_c \tag{14}$$

$$G_{opt} = \sqrt{\frac{G_u}{R_n} + G_c^2} \tag{15}$$

Equation (12) gives us direction as to how to terminate a two port noisy network if we minimize noise figure. Taking this one step further, if we treat a MOSFET as the noisy two-port network, we can express Y_c in terms of MOSFET's characteristic parameters as [26]:

$$Y_c = j\omega C_{gs}\left(1 - \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right) \tag{16}$$

Assuming long channel device, in the above equation, c is -j0.395, α =1, γ = 2/3 and δ = 4/3. We can see that the correlation admittance Y_c is purely imaginary is not equal to the admittance of C_{gs} ($j\omega C_{gs}$). This is also the reason why maximum power gain and minimum noise figure can't be achieved at the same time. We can also see from (16) that source susceptance is inductive so wideband noise match is fundamentally hard to achieve.

Next, two common ways to achieve 50Ω input impedance will be shown.

MOSFET is the workhorse in CMOS technology. In order to amplify a signal, we either feed the signal to the gate (common source structure) or the source (common gate structure). We will explore both of them and see how input matching can be achieved in each case and the challenges with both.

In the common source case, the input impedance is dominated by the gate-to-source capacitance C_{gs}. So it is hard to achieve purely resistive impedance if we don't add extra components. It can be shown that degenerating the source with an inductor can achieve such a goal. If we only consider the MOSFET as a transconductor with gate-to-source capacitance, the input impedance of Fig. 4 can be derived as [26]:

$$Z_{in} = sL + \frac{1}{sC_{gs}} + \frac{g_m L}{C_{gs}} \tag{17}$$

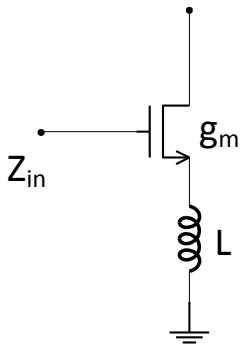

Figure 4. Impedance looking into the gate of inductively degenerated MOSFET.

If we look closely at (17), we can see that it is actually the impedance of a series RLC network. The last term is purely real and by proper biasing and sizing, we can make the resistive part to be 50 Ω. Due to the narrowband characteristic of this RLC networks, this structure needs bandwidth extension techniques if it were to be used in wideband applications which involve the use of multiple inductors and capacitors.

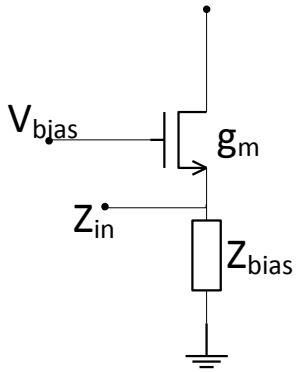

Figure 5. Input impedance of common-gate topology.

In the common gate case (Fig. 5), the input impedance is $(1/g_m)//Z_{bias}$. The MOSFET can be biased by a resistor, an inductor or another MOSFET working as a current source. If resistor is used, there will be DC voltage drop across it which will eat into headroom at the output. However, there will be no frequency dependent term in the input impedance so it is inherently wideband operation. If an inductor is used, there will be a very small DC voltage across it and thus better linearity and lower noise figure but there will be a frequency dependent term in the input impedance which hurts wideband operation. However, we can get around this problem by sizing the inductor so that the impedance is very big compared to $1/g_m$ in the intended frequency range. The use of an inductor consumes larger area than its resistor counterpart. However, the biggest issue common-gate structure faces is that channel noise is large when it is terminated this way.

CHAPTER 3. REVIEW OF LITERATURE

In chapter 2, we discussed several figure of merits of an LNA and the trade-offs involved. In this chapter, we will review literature and see what people have done in the field of ultra-wideband LNA design.

3.1 Distributed Amplifier

Distributed amplifiers are widely used in wideband LNA design [27]-[33]. This type of structure which utilizes several stages of common-source amplifiers is well-known for large power [30]-[32] and area consumption ($0.8mm^2$ in [27] and $1.4mm^2$ in [29]). It combines the parasitic gate-source capacitance with on-chip inductors to build transmission lines which have intrinsic broadband frequency response that goes all the way down to DC [30, 33]. Zhang et al. are able to cut the power consumption to only 9 mw by biasing the MOSFETs in moderate inversion instead of strong inversion [33].

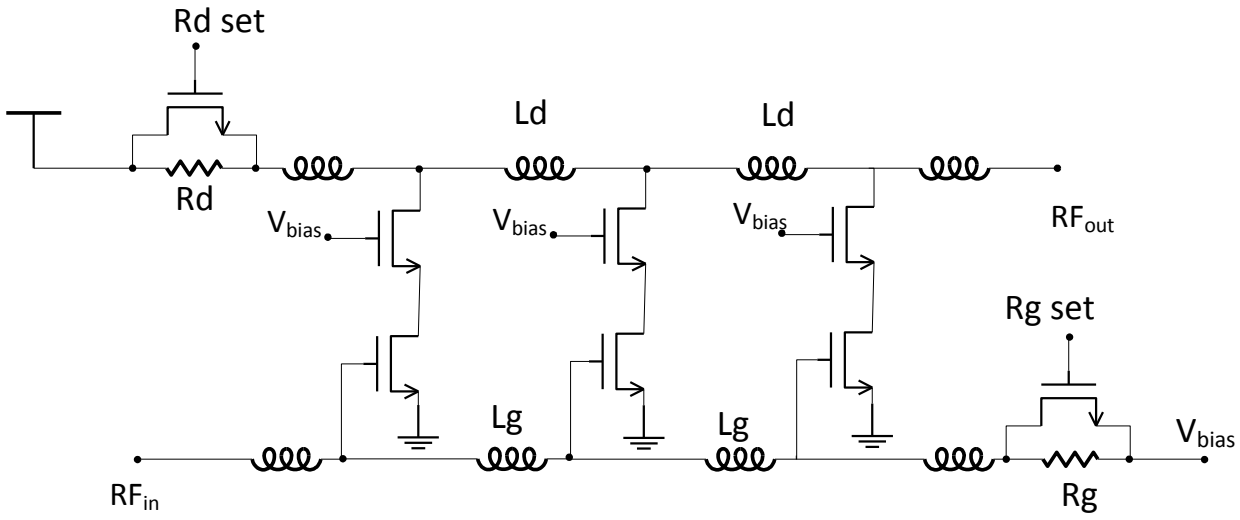

Figure 6. Schematic used in [33].

The schematic used in [33] is shown in Fig. 6. This topology uses so-called pseudo-transmission line to do wideband input and output impedance matching up to its cut-off frequency $1/(\pi RC_g)$ (C_g is the gate capacitance). Pseudo-transmission lines are formed by on-chip inductors and input/output parasitic capacitances. The characteristic impedance of the pseudo-transmission line is $R = (L_g/C_g)^{1/2}$ which can be set to 50 Ω. Components are sized such that the current from different MOSFETs arrive in phase at the output so they interfere constructively with each other. The total power gain is the sum of all stages. However, simply increasing the number of stages will not infinitely increase the gain because the loss in the non-ideal inductors. The signal will be attenuated due to the series resistance of the inductors which will cause the magnitude to drop in latter stages.

Although the authors of this paper were able to cut power to 9 mW, performances like gain (8dB), noise figure (10dB at 7GHz) and area ($1.2mm^2$) are still not very satisfactory.

3.2 G_m Enhancement Technique

Gm boosted technique is another structure commonly used in wideband LNA design [34]-[37]. This type of amplifier typically employs common-gate topology. An inverting gain (A_V) between the source terminal and gate terminals of the CG transistor reduces the power consumption by a factor ($1+A_V$), and leads to a corresponding improvement in noise factor [37].

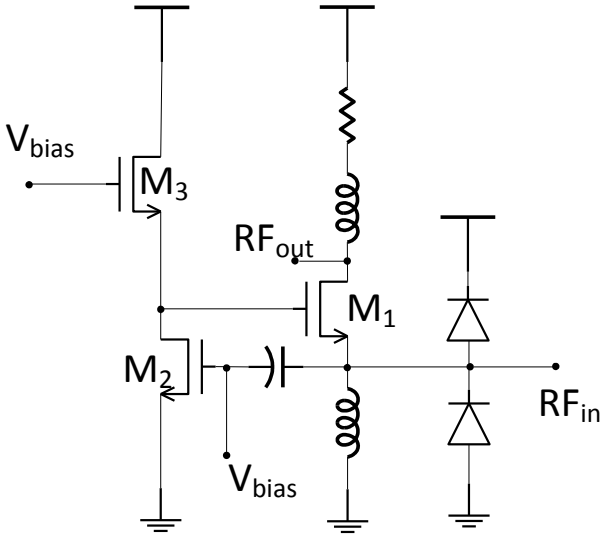

Figure 7. Simplified schematic used in [38].

Shown in Fig. 7 is the schematic of a wideband LNA using Gm enhancement [38]. We can see that this circuit use series R-L as load. The load inductor causes gain peaking at higher frequencies which extends the bandwidth.

Common-gate transistor (M_1) is the basic amplifying transistor. The source inductor is sized such that it has very large impedance in the desired frequency range and has a self-resonant frequency well over 10GHz and provides a current sink for M_1. Tuning the size of M_1 will be needed due the parasitic capacitance seen at the input node. Employing an inductor has better noise performance and adds very little capacitance at the input node compared to using another transistor. Sizing and biasing M_1 around 20mS will provide wideband input match to 50Ω. M_2 and M_3 forms an NMOS based amplifier. This amplifier (voltage gain A_v) is designed to provide g_m enhancement for the common-gate MOSFET (M_1). It can be shown that the effective g_m of M_1 is given by:

$$g_{m,eff} = (1 - A_v)g_m \tag{18}$$

There are several benefits with this g_m enhancement structure. The power gain of the LNA can be increased without too much power overhead if we bias the enhancement circuitry with low current. Another benefit is that the size of the common-gate stage can be reduced significantly and still provide the needed 20mS of transconductance. Smaller size means less parasitic gate-source and gate-drain capacitance, both of which help with wideband operation. The two diodes at the input node are used for ESD protection purposes. They will inevitably introduce parasitic capacitance at the input node and so g_m enhancement seems even more important for ESD protection purposes.

3.3 Band-pass Filter Technique

Next, an example that employs common-source structure will be shown. As discussed in Chapter 1, one way to achieve 50 Ω input matching is done by inductively degenerating the source of the CS transistor. This results in an input impedance that can be modeled as a series RLC network. This technique is inherently narrow-band and hence is unsuitable for wideband applications. However, by incorporating the input of the common-source LNA into a bandpass filter network, where the bandwidth can be independently controlled, the common-source structure can be used in wideband applications. This type of topology is very popular in UWB communications which uses the frequency range of 3.1-10.6GHz. Since cognitive radio also uses frequency range of 1-3GHz so this topology has the problem of not enough bandwidth [1]-[5].

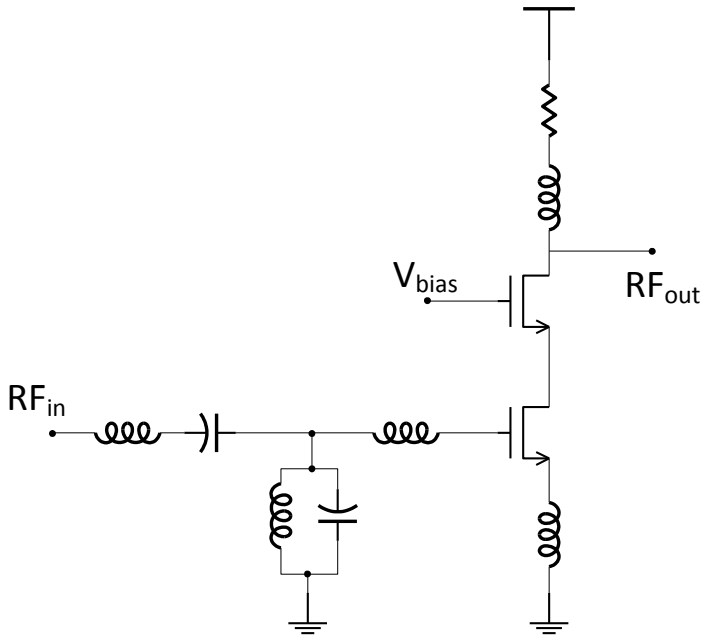

Figure 8. Simplified schematic (buffer omitted) used in [5].

Fig. 8 shows the schematic of a common-source LNA using a band-pass filter input impedance matching network [5]. By embedding the common-source amplifier in to a multisection reactive network, the overall reactance is resonated over a wide frequency range. The output network uses inductive peaking to extend the bandwidth of output impedance. The amplifying stage uses a cascode structure for the purpose of better input-output isolation [1]-[5] and better frequency response [5]. Since this type structure employs common-source topology, the noise performance should theoretically be better than common-gate topology based structures [26]. However, due to the low Q of the input LC network (this is caused by the low Q of on chip inductors), the noise figure is deteriorated [5]. Another drawback is the huge area consumed to build the input band-pass filter (area of [1] is 0.4mm^2, area of [2] is 0.7mm^2).

3.4 Active Inductor

A primary drawback to distributed amplifiers and common-source LNAs using a band-pass filter network is the large area required by the multiple inductors. One way in which to minimize this area is to replace the passive inductors with active inductors [6]-[11]. As discussed in Chapter one, use of active inductor adds additional noise due the active load used. Noise figure achieved in [6] is 5-11dB, [9] is 4-10dB and 3-7dB in [10].

An active inductor can be realized by connecting a MOSFET in such a way that the impedance looking into a terminal increases with frequency.

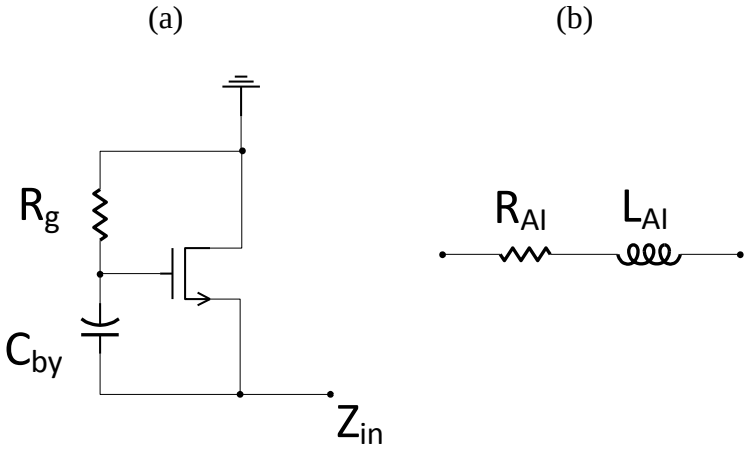

Figure 9. Schematic of (a) an active inductor and (b) the equivalent small signal model

An example of an active inductor is shown in Fig. 9(a) where the gate and source are connected by a capacitor and the drain and gate are connected by a resistor. The impedance looking into the source terminal can be derived as [11]:

$$Z_{AI} = R_{AI} + j\omega L_{AI} \tag{19}$$

where

$$R_{AI} = \frac{1}{g_m} \tag{20}$$

$$L_{AI} = \frac{R_g(C_{gs} + C_{by})}{g_m} \tag{21}$$

We can see from equation (19) that the active inductor is equivalent to a series R-L network (see Fig. 9 (b)). The use of C_{by} is actually optional but having it adds one degree of freedom which makes setting g_m and L_{AI} independently more easily.

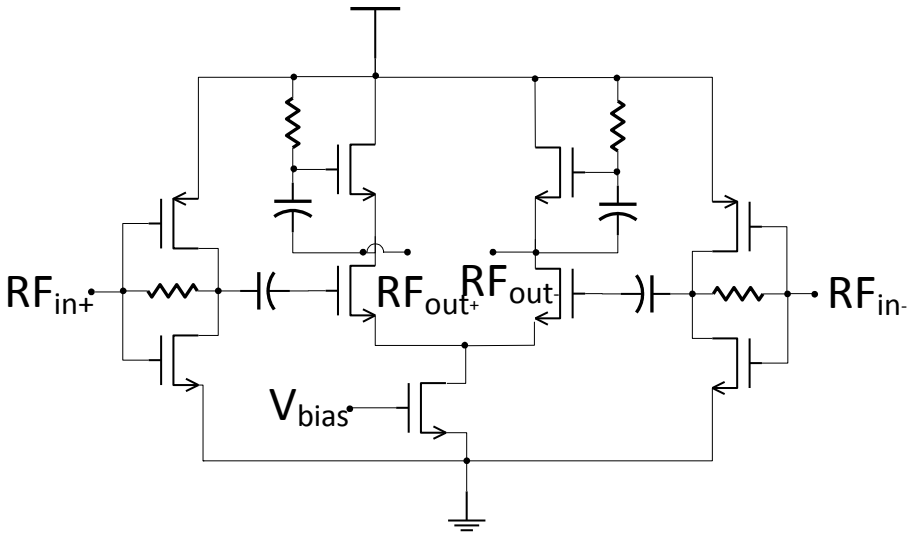

Figure 10. Schematic used in [11].

One notable use of the active inductor is presented in [11]. The schematic used in this paper is shown in Fig. 10. We can see that this LNA uses the first stage which is a self-biased inverter to do wideband input matching. And the second stage is an active inductor loaded common-source amplifier.

We can see that this LNA is differential and it has two stages. One shortcoming single-ended structures have is sensitivity to parasitic ground inductances which may potentially destabilizes the amplifier. Sophisticated packaging and additional ground pins might mitigate such problems but at higher cost. This problem is avoided by using a differential structure [26]. Another advantage that differential LNAs have is the ability to

reject common-mode disturbances. This is especially important in mixed-signal applications because both supply and substrate voltages can be very noisy. However, for fair comparison, if we supply both with the same power, the noise figure of single-ended would be smaller than that of a differential counterpart [26].

3.5 Feedback Technique

In the previous example, we have seen the use of feedback resistor to do wideband input matching. In this section, we will do some analysis on feedback technique and then we will take a look at one example that employs this technique.

The schematic of a shunt-series amplifier is shown in Fig. 11. We can see that the core of the amplifier is consists R_F, R_1 and the transistor. In order to quickly analysis this structure, we will make two reasonable assumptions. First, we assume that $1/g_m$ can be neglected compared to R_1. Second, R_F is big enough that its loading effect on the output node can be neglected. With these two assumptions, we can derive the voltage gain to be $-R_L/R_1$.

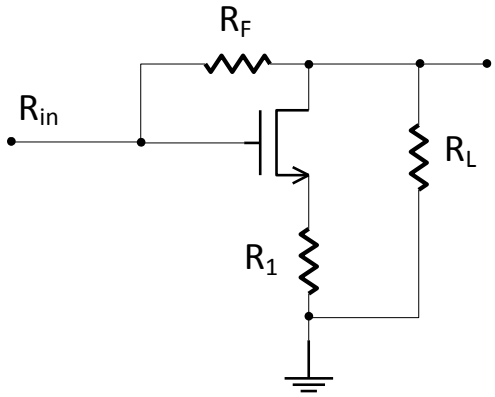

Figure 11. Schematic for shunt feedback amplifier (biasing not shown).

After deriving the gain, input resistance will be discussed. If we neglect the parasitic gate-source capacitance and the current flowing in the gate, this is basically a classic case of Miller effect: connecting two nodes that have an inverting voltage gain (A_v) results in an impedance reduction of ($1-A_v$). Thus R_{in} can be easily derived as [26]:

$$R_{in} = \frac{R_F}{1+\frac{R_L}{R1}} \tag{22}$$

So by properly choosing the values of R_F, R_L, and R_1, wideband input match can be achieved. However, in the context of multi-giga hertz LNA design, the bandwidth of this structure is limited by the input capacitance of the gate. Extra passive components still need to be added to extend the bandwidth. For example [39] uses on-chip inductor to degenerate the source (schematic shown in Fig. 12).

The shunt-feedback structure suffers from trade-off between noise figure and bandwidth. The -3dB bandwidth of shunt-feedback topology is given as [39]:

$$\omega_{-3dB} = \frac{[1+A_v]}{R_f[(C_{gs}+(1+A_v)C_{gd}]} \tag{23}$$

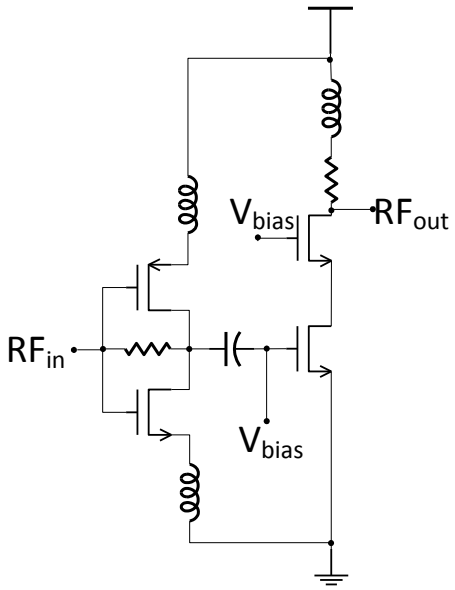

Figure 12. Schematic used in [39].

A_v is the open-loop voltage gain of the amplifier, R_f is the shunt-feedback resistance, and C_{gs} and C_{gd} are gate-source and gate-drain parasitic capacitance. We can see that higher R_f lead to smaller bandwidth but better noise figure (see (18)).

3.6 Feedback Example

One system that utilizes a feedback technique is presented in [40]. The schematic is shown in Fig. 13.

C_1 and C_2 are added for DC decoupling. Input matching is very poorly achieved at lower frequencies because of C_2. L_G and C_{in} are added to compensate for the effect of C_{gs1} to achieve wider bandwidth [40]. A piece of transmission line which gives 50pH is used to degenerate the source. Inductively degenerating the source has been proven to have better linearity and stability [40]. Studies have shown use of transmission line is less prone to

process variation than spiral inductors when the inductance is small [40]. The use of L_P is used to flatten gain response.

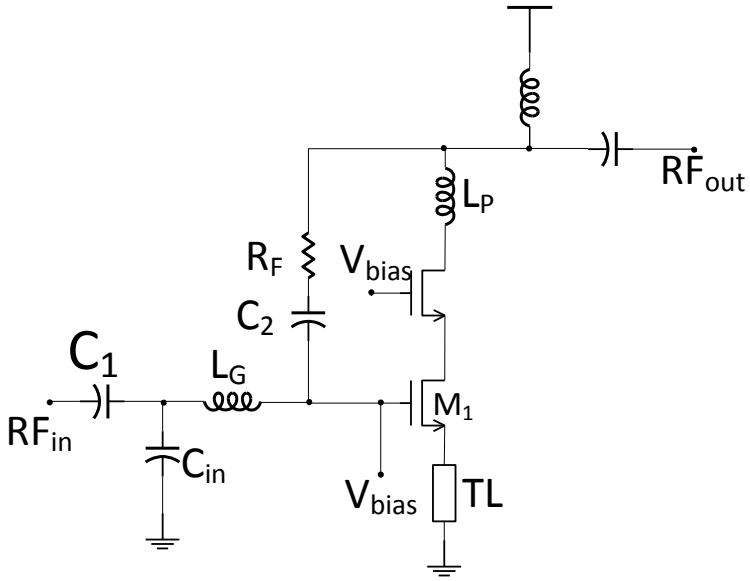

Figure 13. Schematic used in [8].

CHAPTER 4. NOISE-CANCELLATION

It can be concluded from Chapter 2 that using a common-gate structure provides a relatively simple ultra-wideband impedance match that is amenable to implementation using next-generation nanoscale CMOS processes. The drawbacks are slightly reduced gain and higher noise figure. One way that these drawbacks can be mitigated is through the use of noise-cancellation techniques. In this chapter, we will examine how noise-cancellation techniques work and how they can help improve the overall noise figure of ultra-wideband common-gate LNAs. We will also look at several existing designs and see the problems they face and then a new design will be proposed to address these problems.

4.1 Noise-cancelling Technique

In this section, noise-cancellation technique will be discussed. This is also the topology I employed. It should be pointed out that this particular topology is only one out of several noise-cancellation techniques [18]-[20].

The basic idea is as follows: common-gate topology is very suitable for wideband input matching. But the problem is that when $1/g_m$ is matched to 50 Ω, the channel noise of the MOSFET becomes unacceptable large. So in order to combat this problem, we can design another common-source stage which has the same gain. And if we connect them in such a manner that the channel noise show up at both the output node of CG and CS, thus by taking the output differentially the noise will be fully cancelled. We can also get differential output for free which is good for rejecting common-mode disturbances such as supply and substrate noise.

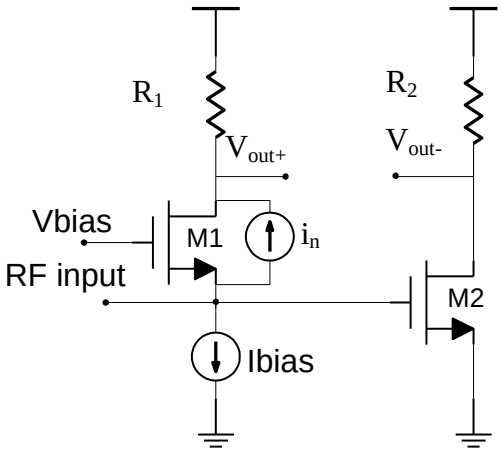

Figure 14. Basic noise cancelling architecture.

A basic noise cancelling architecture is shown in Fig. 14, which consists of two paths: one path consisting of a common-gate amplifier and one path consisting of a common-source amplifier. The noise generated by the common-gate transistor, M_1, can be represented by a current source, i_n. This current generates both a voltage at the input-node ($V_{n,in} = \beta i_n R_S$) and a fully correlated anti-phase voltage at the common-gate output ($V_{n,CG} = -\beta i_n R_1$) where β is the voltage divider ratio between the input resistance ($R_{in,CG}$) and the source (R_s) [21] and is given by:

$$\beta = \frac{R_{in,CG}}{R_S + R_{in,CG}} \tag{24}$$

The noise at the output of the common-source transistor, M_2, is equal to the common-gate output noise. Assuming that the gain of the common-source path is equal to the common-gate path, the thermal noise of transistor M_1 shows up at the differential output as a common-mode signal.

This particular noise-cancelling architecture is advantageous because the input impedance of the common-gate stage is equal to $1/g_{m,M1}$ which can be set to 50 Ω resulting in the broadband impedance match that is required by cognitive LNAs. Moreover, the output of this system is differential. This is desirable as it results in the cancellation of power supply noise, substrate noise, as well as second-order distortion [21]. In addition, differential signals are desirable from the standpoint that most mixer inputs are differential and having a differential LNA output eliminates the need for a balun between the LNA output and mixer input.

4.2 Inductive Series and Shunt Peaking

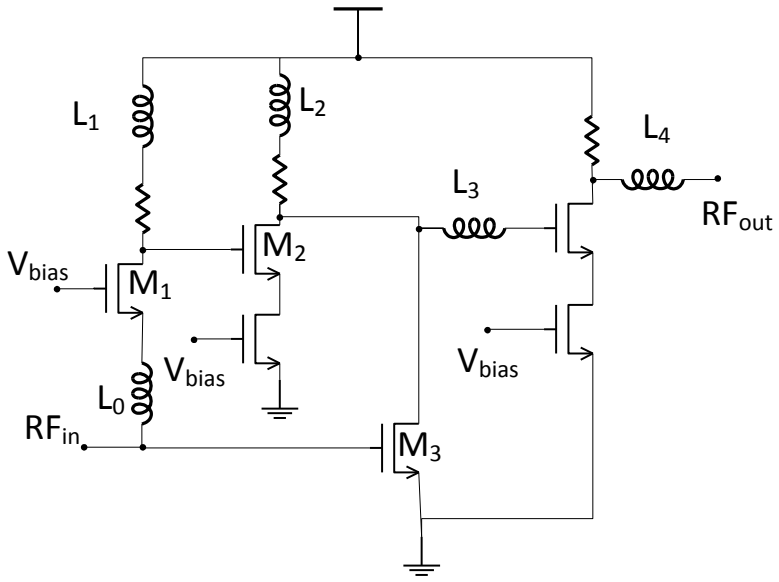

Figure 15. Schematic used in [18].

Liao et al. proposed a system shown in Fig. 15. We can see that this structure produces single-ended output. Noise current from M_1 is cancelled at the drain of M_2/M_3 by a process very similar to that explained in Section 4.1. It uses a total of 4 on-chip inductors

(L_1-L_4) and one off-chip bias inductor L_0 to do both shunt and series peaking to extend the bandwidth. Although this work achieved a very wide bandwidth (1.2-11.9 GHz), the area ($0.59mm^2$), power (20mW) and gain (9.7dB) can be improved.

4.3 Transformer

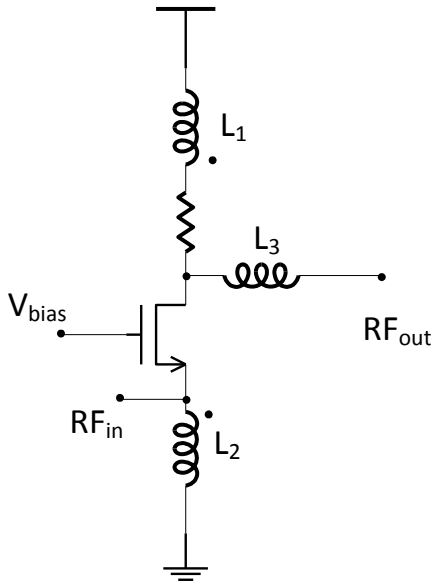

Figure 16. Schematic used in [19].

Very low power (2.5mW) and low noise figure (<3.3dB) is achieved in [19]. We can see that the schematic (Fig. 16) employs 3 inductors and two of them (L_1 and L_2) form a transformer. The transformer partly cancels the output noise voltage produced by the drain noise current of the CG transistor thereby improving the noise performance without additional circuits or power consumption. In order to understand how this structure achieves noise-cancelling, we'll analyze the schematic in Fig. 17 [19].

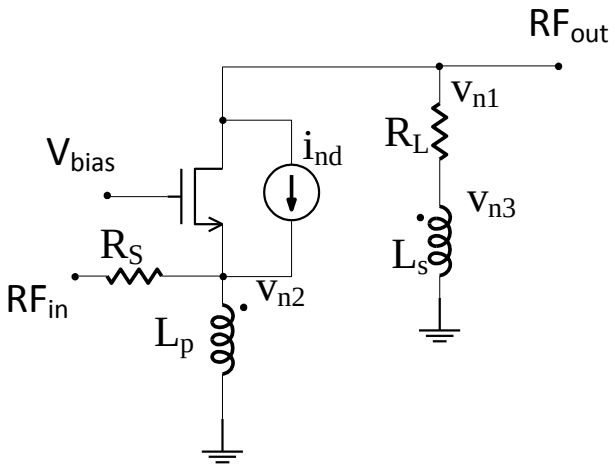

Figure 17. Mechanism for noise cancellation in [19].

The noise current i_{nd} which flows through the secondary inductor L_S and load resistor R_L will generate a noise voltage v_{n1} at output node. The noise current also flows through L_p and R_s which produces another noise voltage v_{n2}. Here, the transformer induces a noise voltage v_{n3}, which is correlated and anti-phase to v_{n1}. In this way, we can see v_{n1} and v_{n3} are partly cancelled at the output.

Although ultra low power and low noise figure is achieved, this works suffers from not enough power gain at higher frequency (7.8 dB).

4.4 Distortion Cancellation

So far we have been talking about cancelling the noise of the common-gate MOSFET. Next, we will take a look at one structure the basic amplifying stage of which is common-source [20]. The full schematic is depicted by Fig. 18.

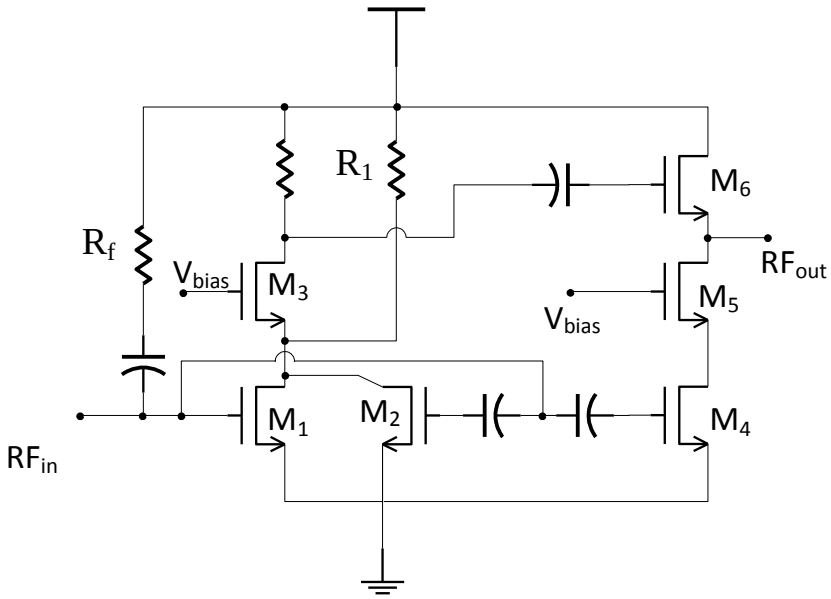

Figure 18. Schematic used in [20].

We can see that wideband input matching is accomplished by the feedback resistor R_f. M_1 and M_3 forms the basic cascode amplifying structure. M_2 is placed in parallel with M_1 for the purpose of 2^{nd} and 3^{rd} order distortion cancellation. R_1 is added to provide one additional degree of freedom for biasing M_2 so that it achieves better distortion cancellation. The current flowing through R_1 will decrease the gain in return for better linearity. The noise at the input node is cancelled at the output node. We can see that the second stage achieves noise-cancelling and signal buffering at the same time.

Although this work achieved superior noise figure (2dB) and linearity (IIP3=2.4dBm), there is still room for improvement in terms of power consumption (30mW) and bandwidth (0.5-5GHz).

4.5 Proposed Ultra-Wideband LNA

To author's knowledge, Blaakmeer et al. [21] achieved the best overall performance (in terms of bandwidth, power consumption, area and noise figure) that employs inductorless differential noise-cancelling topology.

However, the performance needs to be improved if it were to be used in radio communication schemes which are supposed to work beyond 7GHz. The maximum S_{21} is 6.6dB and falls below 4dB beyond 6GHz. S_{11} is higher than -5dB and noise figure is over 5dB beyond 7GHz. My proposed design is meant to address these limitations.

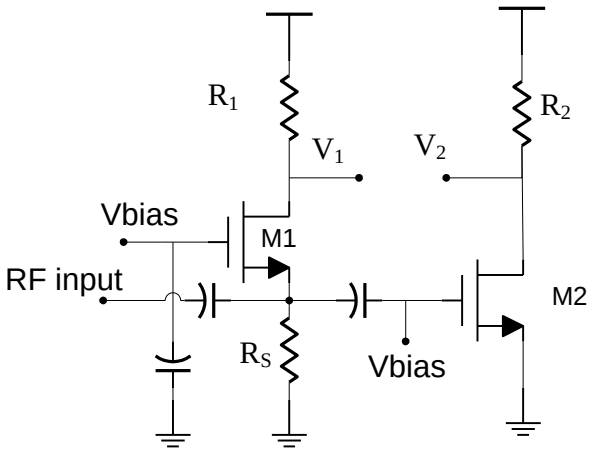

Figure 19. Schematic of the proposed noise-cancelling UWB LNA.

The schematic of the proposed noise-cancelling LNA is shown in Fig. 19 with biasing circuitry omitted. Because the transconductance of transistor M_1 is fixed due to the required input impedance matching, the gain of the overall LNA is limited by the gain of the common-gate stage. In the system proposed in this paper the gain is further limited by the

fact that transistor M_1 is source degenerated by resistor R_S, which must be included for DC biasing purposes. One option for increasing the gain is to increase the load resistor R_1. While initial increases in R_1 does, in fact, lead to an increase in gain, increasing R_1 beyond a certain point results in a reduction in linearity because the dropping DC output voltage pushes M_1 closer to the triode region. The gain of the common-gate stage can be written as:

$$A_{CG} = \frac{R_s}{R_s+R_{source}} \frac{(g_{m1}r_{ds}+1)R_1}{r_{ds}+R_1} \tag{25}$$

where R_{source} is the impedance of the input source and r_{ds} is the drain to source resistance of transistor M_1.

Balancing the linearity, noise figure, and gain requirements, we arrive at the choice of R_1 = 700 Ω and R_S = 200 Ω. Transistor M_1 is biased to give a transconductance of 12 mS, which when placed in parallel with R_s gives an input impedance of approximately 50 Ω. Using (25) the voltage gain of the common-gate stage is calculated to be A_{CG} = 2.45 V/V. A bypass capacitor is placed on the gate of M_1 in order to ensure that no instabilities occur from RF signals leaking back into the biasing circuitry. The biasing resistor was omitted from the gate of M_1 in order to maintain a low noise figure.

As was described in Section 4.1, in order to achieve maximum cancellation of the thermal noise in transistor M_1, the gain of the common-source stage must be matched to that of the common-gate stage. It becomes important to also minimize the noise contribution of the common-source stage. According to [21], the noise contribution from the common-source stage is minimized when the load resistance of this stage, R_2, is 1/4 of the value of the load resistance in the common-gate stage, R_1. It was found through simulation, however, that setting the load resistor of the common-source stage, R_2, to a value of 1/5 that of R_1 was

preferable for this particular case. Setting R_2 = 140 Ω, transistor M_2 can then be biased to give a voltage gain of A_{CS} = -2.45 V/V.

In order to drive a 50 Ω load for testing purposes buffers are required for this design, shown in Fig. 20. The buffers consist of two source followers (chosen for its superior bandwidth performance) that are AC coupled to the output of the common-gate and common-source stages. In order to maximize the linearity and gain of the buffers the inputs are biased at V_{DD} through a resistor (to isolate the RF and DC signals) and care was taken to minimize the parasitic input capacitance as this will directly reduce the bandwidth of the LNA. The differential outputs will be converted to a single-ended output using a standard off-chip balun.

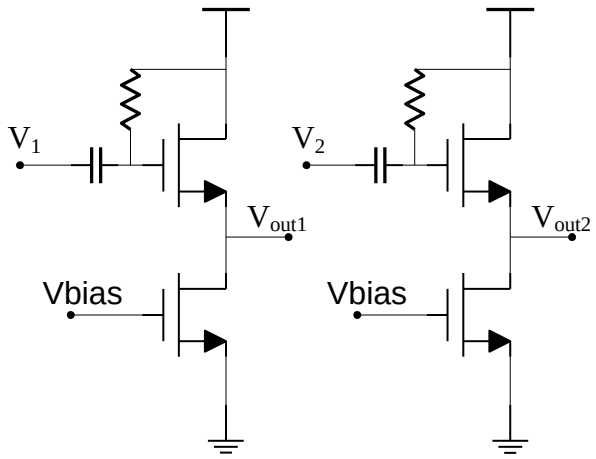

Figure 20. Schematic of the buffer used to drive 50 Ω test equipments.

4.6 Simulation Results

Fig. 21 shows the layout of the proposed LNA. The circuit consumes a total of 140 µm x 220 µm (0.03mm^2) excluding the pads. It is seen that over 90% of the area is consumed by the AC coupling capacitors owing to the poor scaling of passive devices.

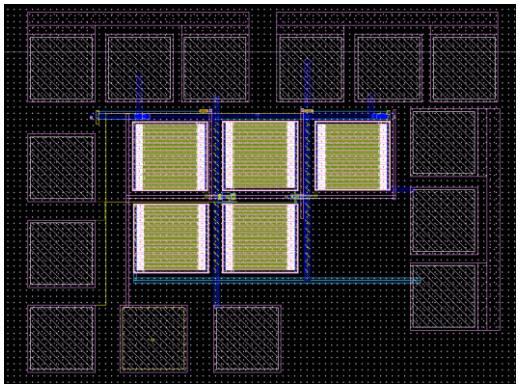

Figure 21. Final layout of the noise-cancelling UWB LNA. The circuit consumes a total of 140 µm x 220 µm excluding the pads.

Post layout simulations were performed using extracted resistance and capacitance and were performed over the typical, fast, and slow corners. Fig. 22 and Fig. 23 show the simulated S_{11} and S_{21}, respectively. For the typical corner, S_{11} is below -10 dB across the frequency range of 2.5 GHz to 6 GHz. If the requirement on S_{11} is relaxed by 0.5 dB to -9.5 dB, the bandwidth of this amplifier expands to a range of 1.5 GHz to 9.5 GHz across all corners. Over the range of 1.5-9.5 GHz, and across all corners, the maximum and minimum S_{21} is 14 dB and 9 dB, respectively.

The simulated noise figure is shown in Fig. 24. It is seen that the maximum noise figure occurs at 9.5 GHz for the fast corner and the value is a respectable 4.3 dB. Finally the linearity is simulated at multiple frequencies between 1 GHz and 10 GHz. The results are plotted in Fig. 25. The simulated IIP3 is approximately 0 dBm and it is relatively flat across

the entire range of frequencies. Finally, the simulated DC consumption was simulated and it was found to be 8 mW for the LNA core, neglecting the power consumed by the buffers. Table I shows compares the performance of this system to that of similar LNAs published in the literature.

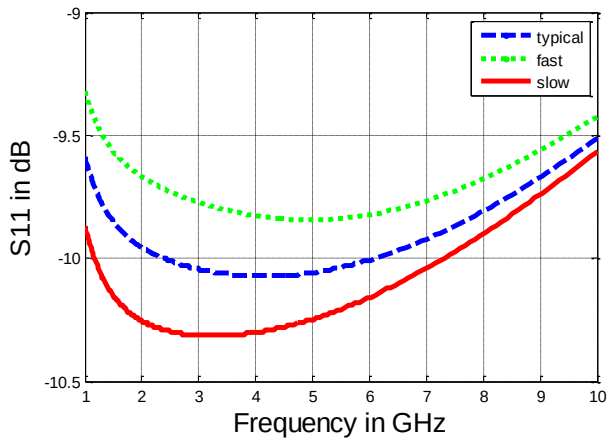

Figure 22. Simulated S_{11}showing a bandwidth of 1.5 GHz to 10 GHz.

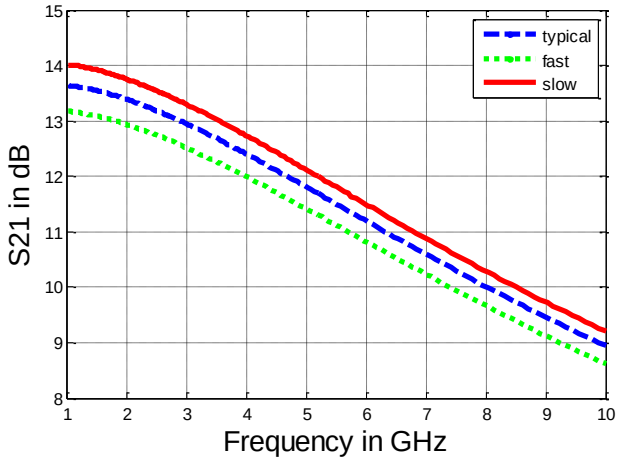

Figure 23. Simulated S21 showing a minimum gain of 9 dB.

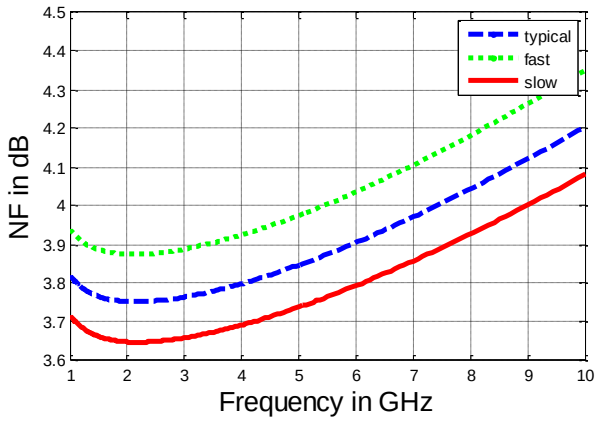

Figure 24. Simulated noise figure showing a maximum noise figure at 9.5 GHz of 4.3 dB.

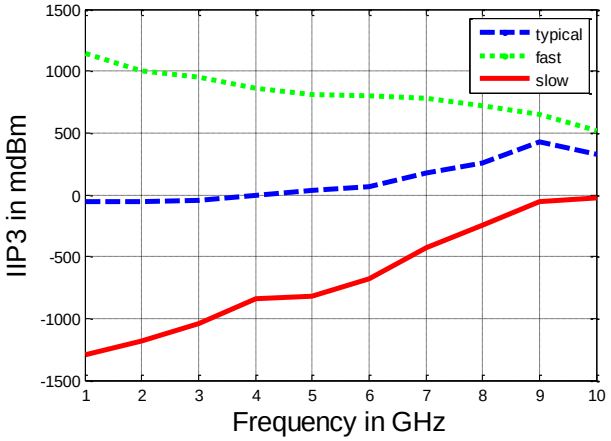

Figure 25. Simulated IIP3.

Table I

Ref	Bandwidth [GHz]	NF [dB]	S21 [dB]	S11 [dB]	IIP3 [dBm]	Power [mW]	Area [mm^2]	Feature Size[nm]	meas
This work	1.4-9.5	<4.3	9-13	< -9.5	0	8	0.03	40	sim
Blaakmeer	0.2-5.3	3.5	6.6	< -10	0	21	0.009	65	fab
Hampel	1-10.5	4-5	< 16.5	< -10	-5	36	0.02	65	fab
Liao	3.1-10.6	4.5-5	<10	< -10	-6.2	20	0.6	180	fab
Kihara	3.1-14	2.7-3.3	8-12	< -10	-6.4	2.5	0.1	90	fab
Najari	1-5	<2	<11	< - 11	2.4	30	NA	90	sim
Bevilacqua	0.6-22	4.2	<10.4	< -9.4	-8.8	9	1.1	180	fab
Zhang	0-6.2	4.2-6.2	7.4-8.6	< -16	3	9	1.16	180	fab
Bhatia	1.7-11.6	3.1-4	<15.4	< -6	-11.2	8	0.5	180	fab

Note: sim=simulated, fab=fabricated.

CHAPTER 5. COGNITIVE RADIO

In the previous chapters, we have looked at the design of ultra-wideband LNA which is part of the cognitive radio front-end. In this chapter, cognitive radio communication scheme will be discussed. Later in the chapter we will see a proposed spectrum sensing technique which aims at maximizing the data throughput of the cognitive radio.

5.1 Introduction to Cognitive Radio

Cognitive radio is a type of wireless communication paradigm in which the transceivers can intelligently change its transmission or reception parameters based on actively monitoring the parameters in the external and internal radio environment. These parameters may include carrier frequency, signal bandwidth or transmitting power.

Conventional radios are designed to operate within a narrowband of interest. These bands, which are normally called licensed bands, are allocated by regulatory bodies such as the FCC. With so many new wireless standards emerging, the radio frequency range of 1-10 GHz is quickly becoming saturated.

Moving beyond 10 GHz will have the advantage of more available bandwidth. However, high path loss associated with higher radio frequencies limits the communication range to a few meters. Moving below 1 GHz has the problem of lower bandwidth thus lower data rate and unacceptably large antenna size. So 1-10GHz is the “golden range” to implement wireless devices with current CMOS technologies.

Regulatory bodies in various countries (including the FCC in the United States and Ofcom in the United Kingdom) found that most of the radio frequency spectrum was

inefficiently utilized. For example, in 2002, a study done by FCC found that the actual use of spectrum in USA varies from 15% to 85% depending on the place and time of day. Another study done in downtown Chicago showed that the average spectrum usage over the measurement period from November 16-18, 2005 was only 17.4% [41]. This inefficient use of spectrum is the basic problem cognitive radio technology tries to solve.

Similar to the idea of dynamic host configuration protocol (DHCP) which dynamically allocate IP addresses to different users, cognitive radio dynamically allocate unused bands to different users.

One important thing we need to realize is that cognitive radio users (which we call secondary users) do not have primary rights to use those licensed bands. So cognitive radio technology must be implemented in a way such that secondary users do not affect users who have primary rights to the licensed bands (which we call primary users).

Primary users might come online at any time so secondary users must be able to detect their presence immediately and change its own carrier frequency to another available band. So cognitive radios need to constantly be aware of what frequency range is not occupied (spectrum holes). This is accomplished by spectrum sensing which is performed over the entire bandwidth where the cognitive radio is able to operate.

Cognitive radio has the advantage of using spectrum much more efficiently. However, the overhead associated with spectrum sensing can be problematic. The bandwidth needed to do spectrum sensing directly reduce data throughput and in some cases stop data communication altogether.

5.2 Spectrum Sensing

Previous research on the topic of spectrum sensing has focused on systems that perform spectrum sensing and communication separately, or if they perform such operations simultaneously it is through using two parallel RF front-ends [23]. There is a high cost in terms of die area and power consumption associated with duplicating the entire RF front end. Combined with the need for two flexible band-select filters and a dedicated antenna for spectrum sensing, this solution is unfeasible for handheld mobile applications.

Another solution was to use multiple antennas at the receiver [42], [43]. Each separate antenna could sense a different band of frequencies resulting in a parallel approach to spectrum sensing [42]. By performing the sensing in parallel the overall sensing time can be reduced by a factor equal to the number of antennas. However, in order for this system to operate from 1 – 10 GHz, multiple band-select filters would be required.

In this thesis, I will propose a new spectrum sensing algorithm that will facilitate simultaneous spectrum sensing and data reception using one front-end while eliminating the need for multiple band-select filters.

5.3 Translational Loop

In many wireless standards, the receiver must satisfy certain blocking template defined at various frequencies and power levels. For example, in the Global System for Mobile Communications (GSM) standard, a desired signal that is only 3 dB above the sensitivity can be accompanied by an out-of-band blocker as large as 0 dBm which is only 80 MHz away [44]. So we need the gain of the LNA to be high due to the low power of desired

signal and this means the blocker has to be significantly attenuated before it reaches the LNA because of the finite linearity of the LNA. However, due to the poor quality factor of on-chip inductors, it is very hard to implement filters with such sharp frequency response. This is why nearly all current receivers have an external surface acoustic wave (SAW) filter at the input of the LNA.

The use of these SAW filters has several disadvantages: 1) the insertion loss (around 2-3 dB) will degrade the noise figure of the receiver; 2) more filters (thus higher cost) will be needed for multiband applications; 3) makes the sharing of LNA impossible.

The reason why we need high Q inductors is that Q is proportional to center frequency ($Q=f_0/\Delta f$). So if we can translate the frequency down to DC or near DC to get needed filtering done and translate the frequency back up, we can eliminate the use of SAW filters [44]. In the next section, we will discuss the use of translational loop which employs this idea.

In order to understand how translational loops works, the block diagram described by Fig. 26 will be analyzed. Before any derivation, we make the assumption that all blocks in the diagram are linear and time-invariant (LTI) systems.

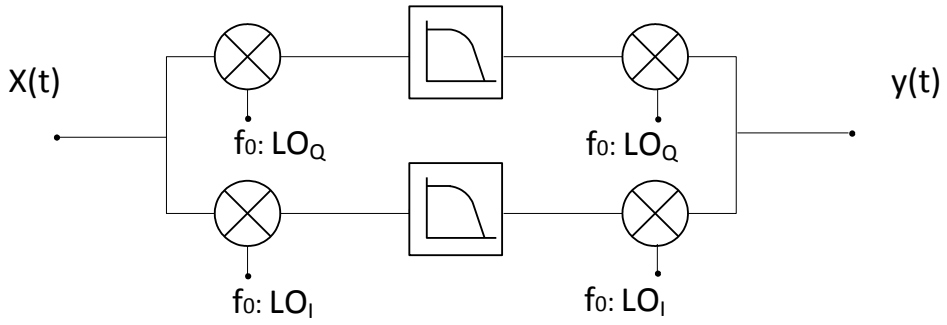

Figure 26. Block diagram used for understanding translational loops

In (26) to (29), x(t) is the input signal, y(t) is the output signal, h(t) is the impulse response of the baseband filter, f_0 is the local oscillator (LO) frequency.

$$y(t) = \{[x(t)\cos(2\pi f_0 t)] \otimes h(t)\} \times \cos(2\pi f_0 t) + \{[x(t)\sin(2\pi f_0 t)] \otimes h(t)\} \times \sin(2\pi f_0 t) \quad (26)$$

$$y(t) = \int [x(\tau)h(t-\tau)][\cos(2\pi f_0 t)\cos(2\pi f_0 \tau) + \sin(2\pi f_0 t)\sin(2\pi f_0 \tau)]d\tau \quad (27)$$

$$y(t) = \int x(\tau)[h(t-\tau)\cos(2\pi f_0 (t-\tau))]\, d\tau \quad (28)$$

From (26) to (28) we can draw the conclusion that the equivalent impulse response (H(t)) of the RF filtering path can be expressed as (29).

$$H(t) = h(t) \times \cos(2\pi f_0 t) \quad (29)$$

Hence, in the frequency domain, the frequency response of the RF filtering path is basically that of the baseband filter but translated to f_0. Thus, by using this structure, very sharp filtering can be easily achieved without the need of high Q on-chip inductors. One other benefit is that the bandwidth can be made variable by using variable resistor or capacitor.

5.4 Simultaneous Spectrum Sensing and Data Reception

In the last section, we looked at a structure that can achieve sharp band-select at very high frequency by moving the signal to DC and then moving it back to RF. This will replace the expensive and inflexible SAW filter with single pole filter low-pass filter (LPF).

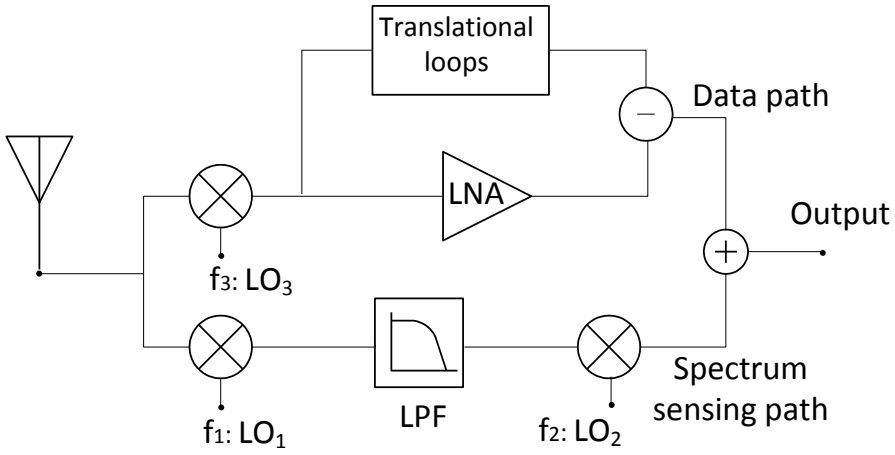

Figure 27. Proposed spectrum sensing RF front end

Shown in Fig. 27 is the proposed spectrum sensing front end. We can see that it has two paths: 1) data reception path and 2) spectrum sensing path. We can see that the data reception path also has a translational loop as well. This baseband filter of this loop is a high pass filter which is designed to pass the blocker and eliminate desired signal. And by subtracting at the output of LNA, blocker will be removed.

Now let's take a look at the spectrum sensing path. There are 3 parameters involved in this path: f_1, f_2 and bandwidth (BW) of the LPF. From the analysis in section 8.2, it should be clear that f_1 is the center frequency around which we would like to perform spectrum sensing and the bandwidth of the LPF will dictate the frequency range (i.e. f1±BW is the

range). For example, suppose a cognitive radio is interested in whether the frequency range of 2.426GHz – 2.448GHz (this is the 6th channel of WLAN G-band) is occupied or not, I would make f_1 to be 2.437GHz and BW to be 11MHz.

The frequency f_2 is the center frequency which I would like to be moved back to. We are certainly not obligated to move if back to its original frequency (f_1) so this is one more degree of freedom that we have. Since we would like to achieve simultaneous data reception and spectrum sensing at the same time, we can place it side-by-side with the data signal in the frequency domain. In this way, we can treat the summed signal as one signal which can be processed by one radio.

In summary, the spectrum sensing front end achieves the function of removing the blocker and moving the spectrum sensing signal close to data signal which can be summed up and treated as one signal. And the reason we prefer moving spectrum signal closer to the data signal instead of where it was is to minimize the bandwidth and power of the following radio. For instance, if a cognitive radio is operating at 5GHz and it is doing spectrum sensing at 1GHz. If we don't move it around 5GHz, the radio will need to process 4GHz of bandwidth. This will also demand very fast A/D converter after the radio front end which burns a lot of extra power.

5.5 Simulation Results

In this section, simulation results from Simulink will be presented. Shown in Fig. 28 is the block diagram used to simulate blocker removal. As stated previously, blocker can be as close as 80MHz away so I made signal to be at 1GHz and blocker to be at 1.08GHz.

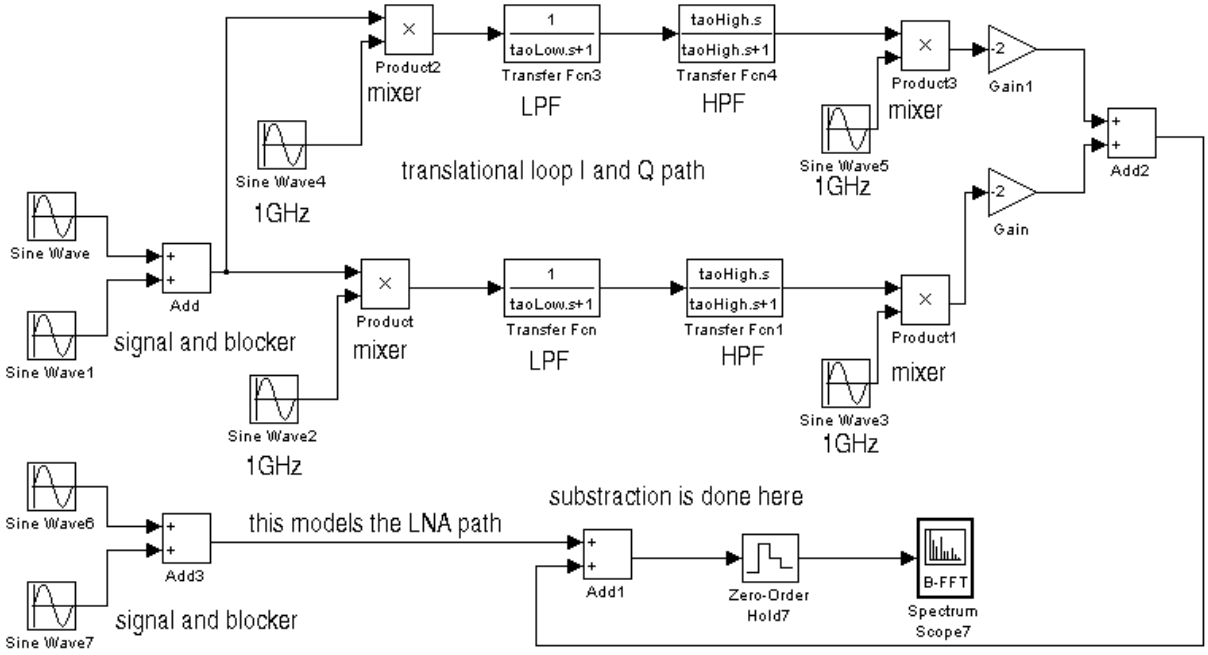

Figure 28. Block diagram used to demonstrate blocker removal.

We can see that there are two paths in the above diagram. One path is the LNA path which simply amplifies the signal. The other path is the translational loop path. From the analysis of previous section, we know the output is of this path is the blocker. So when these two output signals get subtracted at the output of the LNA, blocker will be removed leaving only the desired signal at 1GHz.

The LPF is used to model the low pass characteristics of the building blocks such as the mixer. Mixers are modeled by a product block which multiplies two input signal in the time domain. The pole of the HPF is picked to be 60MHz which is 20MHz away from the blocker. There is a gain of 2 at the output of I/Q path. This boost is needed due to lost of signal power in mixing. We can see from Fig. 29 and Fig. 30 that there is a good 30dB of rejection on the blocker by using single pole LPF.

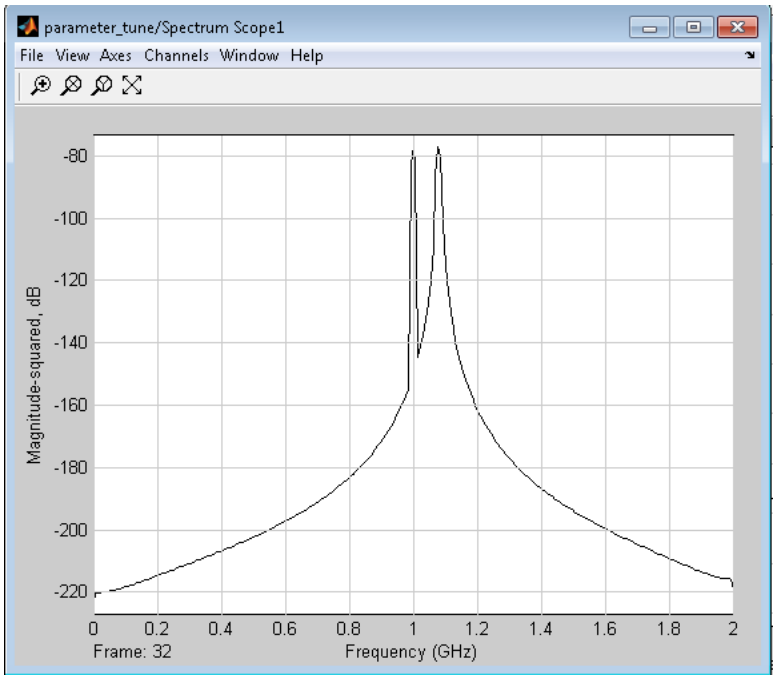

Figure 29. Spectrum of the input signal.

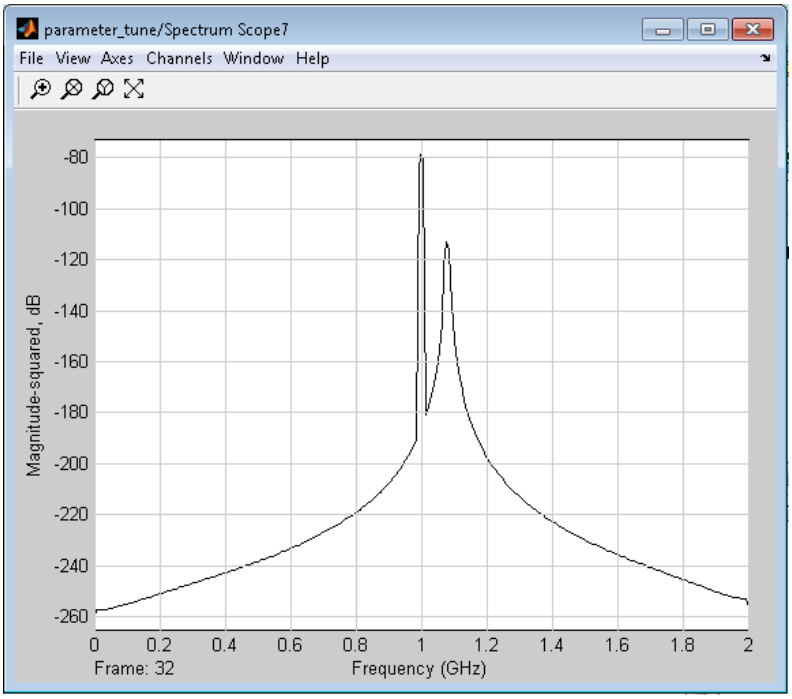

Figure 30. Spectrum of the output signal

We have demonstrated the use of translational loop to remove blockers previously, now we will demonstrate such use for spectrum sensing purposes.

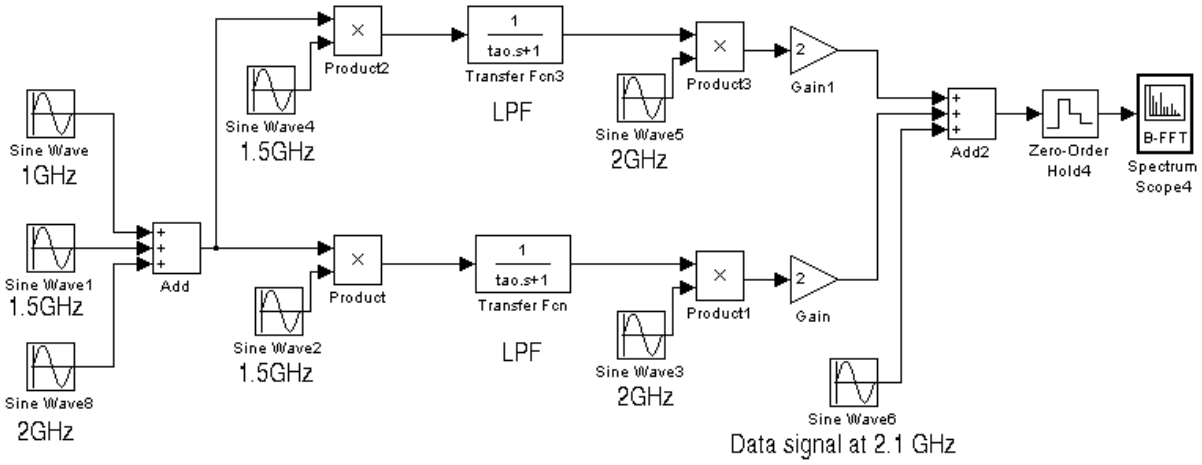

Figure 31. Block diagram used to demonstrate band-select using translational loop

In Fig. 31, we have shown the block diagram used to simulate spectrum sensing. The input of the spectrum sensing front end is consisted of 3 tones: 1GHz, 1.5GHz and 2GHz (Fig. 32). In this case, we are interested in knowing whether the band around 1.5GHz is available or not so we make the LO of the first mixer to be 1.5GHz. We assume the data communication is being done at 2.1GHz so we make the LO of the second mixer to be at 2GHz. Final spectrum is demonstrated in Fig. 33.

Thus we can see the method of using translational loops to achieve spectrum sensing is verified by Simulink. This type of front-end will eliminate the use of expensive SAW filters and can achieve the function of moving spectrum sensing signal close to data signal.

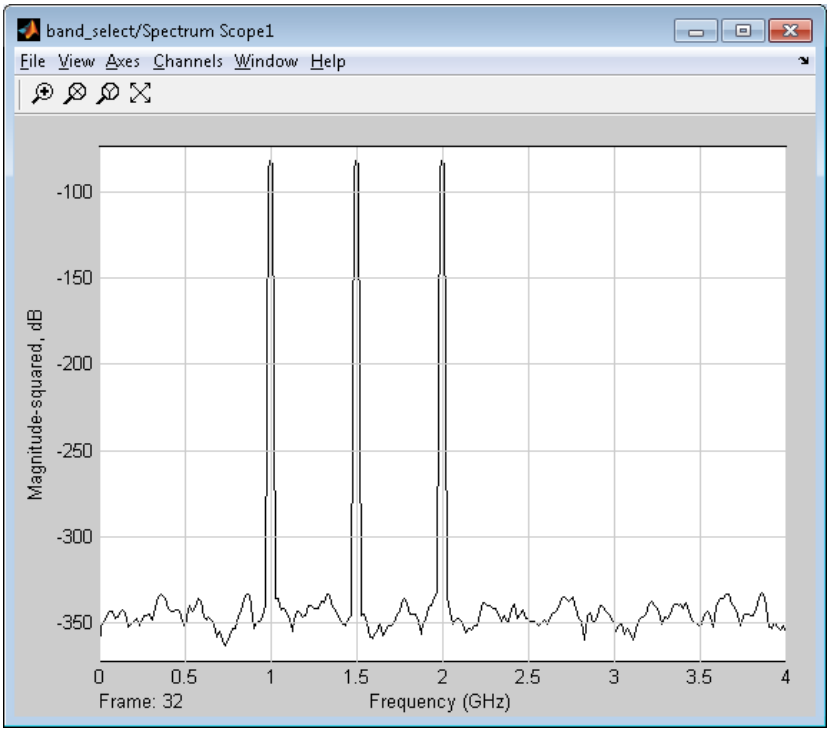

Figure 32. Spectrum of the input signal fed into the spectrum sensing front end

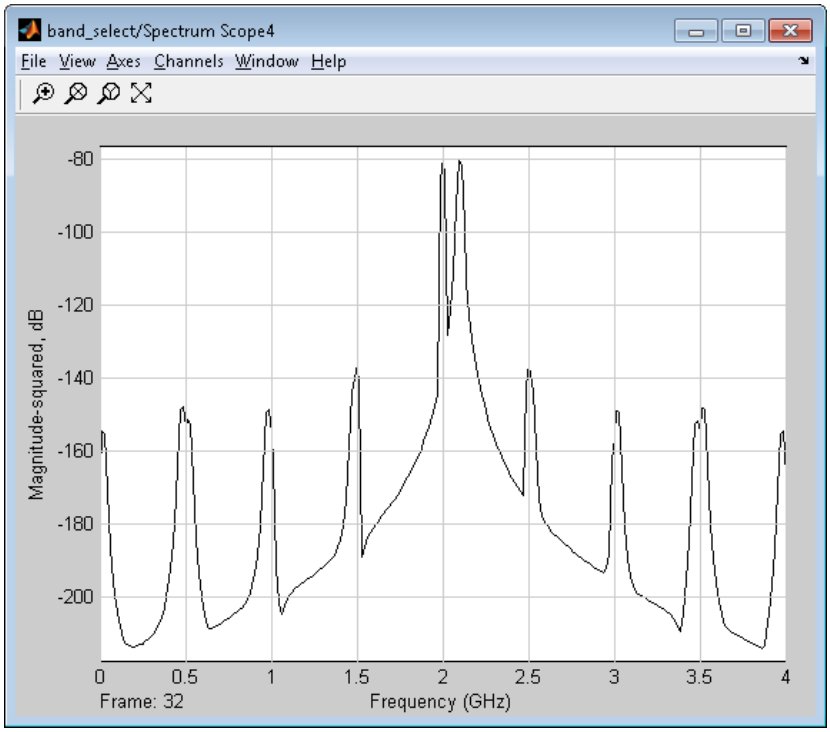

Figure 33. Spectrum of the data signal and spectrum sensing signal

CHAPTER 6. FUTURE WORK

More than 2dB of S_{21} was lost at 10GHz in post-layout simulation compared to initial schematic simulation. The author believes spending more time and effort in better layout design will result in smaller lost in power gain at higher frequencies.

In modern CMOS transceiver architecture, the LNA normally drives a mixer which will present a slightly different loading condition than the buffer that is currently used to drive 50Ω test equipment. It is expected that some tuning of the sizing and biasing will be needed if this LNA were to be integrated into a full transceiver.

The wideband LNA is only part of the spectrum sensing front-end (see Chapter 8 for more detail). The full front-end also requires wideband mixers and phase-locked loops which can be carried in later phase of the project.

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